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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,761	08/14/2003	MING-SUNG SHIH	9886-US-PA	1760
31561	7590	08/23/2004	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE			ISAAC, STANETTA D	
7 FLOOR-1, NO. 100			ART UNIT	
ROOSEVELT ROAD, SECTION 2			PAPER NUMBER	
TAIPEI, 100			2812	
TAIWAN			DATE MAILED: 08/23/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/604,761	SHIH, MING-SUNG
	Examiner Stanetta D. Isaac	Art Unit 2812 <i>pw</i>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 August 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-18 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.



LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 8/14/03. Currently, claims 1-18 are pending.

Specification

The disclosure is objected to because of the following informalities: In paragraphs [0031], lines 11 and 13, and [0036], lines 9 and 11, the specification discloses “ions/cm²” as the units for concentration, however the units for concentration should be “ions/cm³”. For examination purposes on the merits, the Examiner has regarded “ions/cm²” as a typographical error. Appropriate correction is required.

Claim Objections

Claim 13 is objected to because of the following informalities: In line 23, the limitation “san” should be “an”. For examination purposes on the merit, the Examiner has regarded “san” as a typographical error and, has examined the claim as if the limitation reads “an”. Appropriate correction is required.

Claims 5, 12, and 18 are objected to because of the following informalities: In lines 2 and 4, respectively, the limitation shows “ions/cm²” as the units for concentration, instead the units for concentration should be “ions/cm³”. For examination purposes on the merits, the Examiner has regarded “ions/cm²” as a typographical error and, has examined the claims as if the limitation reads “ions/cm³”. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13-18 recites the limitation "the polysilicon layer" in line 6, of independent claim 13. There is insufficient antecedent basis for this limitation in the claim.

The limitation "the polysilicon layer", in claim 13, lacks antecedent basis, in that it does not appear to be disclosed anywhere in the specification that the mask is set above the polysilicon layer. The specification only discloses setting the mask above the photoresist layer. Therefore, for the purpose of examination, on the merits, the Examiner has regarded "the polysilicon layer" as the "photoresist layer".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukata et al. US Patent 6,452,241 in view of Somekh et al. US Patent 4,231,811.

Fukata shows the semiconductor method substantially as claimed. See figures 1-9, and corresponding text, pertaining to claims 1, 6, and 13, where Fukata shows a method of forming an LDD of a polysilicon TFT, comprising: providing a substrate 1 having a polysilicon layer 31 (figure 9, patterned polysilicon layer) thereon, wherein the polysilicon layer comprises a first region 6 and second region 7, 8; performing an ion implantation step using a mask for simultaneously forming source/drain in the first region of the polysilicon layer and an LDD in the polysilicon layer underneath the edge portion (figure 9; col. 8, lines 40-45). In addition, Fukata shows, pertaining to claims 4 and 11, the method wherein, the step of forming the

polysilicon layer comprises: forming an amorphous silicon layer 31 on the substrate (col. 6, lines 10-15); and performing a laser annealing process for transforming the amorphous silicon layer to a polysilicon layer (col. 6, lines 10-15);

However, Fukata fails to show, pertaining to claims 1, 6, and 13, forming a photoresist layer on the polysilicon layer; setting a mask above the photoresist layer, wherein the mask comprises a non-exposing region, an exposing region, and a partial-exposing region; performing a photolithography and etching process for forming a patterned photoresist layer for exposing the first region and covering the second region, wherein the patterned photoresist layer covering the second region comprises a middle portion and an edge portion, and wherein the middle portion is thicker than the edge portion; and performing an ion implantation step using the photoresist layer as a mask. In addition, Fukata fails to show, pertaining to claims 2, 3, 9, 10, 16, and 17, the method wherein the thickness of the middle portion of the photoresist layer is about 1 to 5 μm and the thickness of the edge portion of the photoresist layer and the width of the LDD is about 0.1 to 1 μm . Fukata also fails to show, pertaining to claims 5, 12, and 18, the method wherein the ion concentration in the source/drain is about 1×10^{14} to 1×10^{15} ions/cm³, and the ion concentration in the LDD is about 1×10^{12} to 1×10^{14} ions/cm³. Finally, Fukata fails to show, pertaining to claims 7, 8, 14 and 15, the method wherein the partial-exposing region of the mask comprises a pattern of a plurality of long strips having a width of the long strips and a distance between two adjacent long strips of about 0.05 to 0.5 μm .

Somekh teaches in figures 1-6, and corresponding text, in similar semiconductor method, including a photoresist and mask technique, pertaining to claims 1, 6, and 13, setting a mask 32a-c above the photoresist layer, wherein the mask comprises a non-exposing region 32a, a

exposing region **32c**, and a partial-exposing region **32b**; forming a patterned photoresist layer on the polysilicon layer for exposing the first region and covering the second region (figure 5), wherein the patterned photoresist layer covering the second region comprises a middle portion **34a** and an edge portion (col. 4, lines 24-27), and wherein the middle portion is thicker than the edge portion (col. 4, 18-23); and performing an ion implantation step using the photoresist layer as a mask (col. 4, lines 27-30). In addition, Somekh teaches, pertaining to claims 2, 3, 9, 10, 16, and 17, the method wherein the thickness of the middle portion of the photoresist layer is about 1 to 5 μm and the thickness of the edge portion of the photoresist layer is about 0.1 to 1 μm (col. 4, lines 18-23). Finally, Somekh teaches, pertaining to claims 7, 8, 14 and 15, the method wherein the partial-exposing region of the mask comprises a pattern of a plurality of long strips having a width of the long strips and a distance between two adjacent long strips of about 0.05 to 0.5 μm (col. 2, lines 63-64).

It would have been obvious to one of ordinary skill in the art to have replaced the masking technique, shown in Fukata, by setting a mask above a photoresist layer, wherein the mask comprises a non-exposing region, a exposing region, and a partial-exposing region; and to have formed a patterned photoresist layer on the polysilicon layer for exposing the first region and covering the second region, wherein the patterned photoresist layer covering the second region comprises a middle portion and an edge portion, and wherein the middle portion is thicker than the edge portion; and to have performed an ion implantation step using the photoresist layer as a mask, in the method of Fukata, pertaining to claims 1, 6, and 13, according to the teachings of Somekh, with the motivation that, as stated in Somekh, shown in figures 3-5; abstract; col. 1, lines 36-41; col. 2, lines 18-30; col. 4, lines 1-30, the self-aligned single masking technique

taught by Somekh, is used to improve misalignments that result from conventional two masking techniques used in photolithographic fabrication. In addition, the self-aligned single masking technique, also helps improves cost-efficiency and high production processing of semiconductor devices. Finally, one of ordinary skill in the art would use the self-aligned single mask technique, for the purpose of creating a more defined LDD region profile.

It would have been obvious to one of ordinary skill in the art to incorporate, the thickness of the middle portion of the photoresist layer being about 1 to 5 μm and the thickness of the edge portion of the photoresist layer being about 0.1 to 1 μm , in the method of Fukata, pertaining to claims 2, 3, 9, 10, 16, and 17, according to the teachings of Somekh, with the motivation that, as stated in Somekh, col. 4, lines 18-23, the thickness of the middle and edge portion of the photoresist layer, are about 1 and 0.5 μm , respectively. Therefore, one of ordinary skill in the art would use the claimed thickness, being reasonable in range, for the purpose of aligning the photoresist layer edges to perform a single mask technique including an ion implantation method to form the source/drain regions.

It would have been obvious to one of ordinary skill in the art to incorporate, the partial-exposing region of the mask comprising a pattern of a plurality of long strips having a width and a distance between two adjacent long strips of about 0.05 to 0.5 μm , in the method of Fukata, pertaining to claims 7, 8, 14 and 15, according to the teachings of Somekh, with the motivation that, as stated in Somekh, col. 2, lines 63-64, the width of the long strips is about 0.4 μm wide and the strips are separated by 0.4 μm spaces, as a result, one of ordinary skill in the art would conclude that the claimed ranges are reasonable. The purpose of the spacing is to decrease the intensity of the illumination process in order to vary the thickness of the photoresist layer.

It would have been obvious to one of ordinary skill in the art to incorporate, the method wherein the ion concentration in the source/drain is about 1×10^{14} to 1×10^{15} ions/cm³, and the ion concentration in the LDD is about 1×10^{12} to 1×10^{14} ions/cm³, pertaining to claims 5, 12, and 18, in the method of Fukata, based on the combined Fukata in view of Somekh, with the motivation that, both methods are performed under the use of conventional techniques, resulting in the formation of the source/drain and LDD regions using ion implantation techniques. The claimed ion concentrations of the source/drain and LDD regions are considered to be within conventional specifications, especially since no criticality has been shown.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
August 11, 2004


LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812